Microsemi
POWER PRODUCTS GROUP

Power MOS 8
Cooler!™

N-Channel MOSFET

Power MOS 8™ is a high speed, high voltage N-channel switch-mode power MOSFET. A proprietary planar stripe design yields excellent reliability and manufacturability. Low switching loss is achieved with low input capacitance and ultra low C_{rss} "Miller" capacitance. The intrinsic gate resistance and capacitance of the poly-silicon gate structure help control slew rates during switching, resulting in low EMI and reliable paralleling, even when switching at very high frequency. Reliability in flyback, boost, forward, and other circuits is enhanced by the high avalanche energy capability.

TO-247

D³PAK

APT18M100B   **APT18M100S**

Single die MOSFET
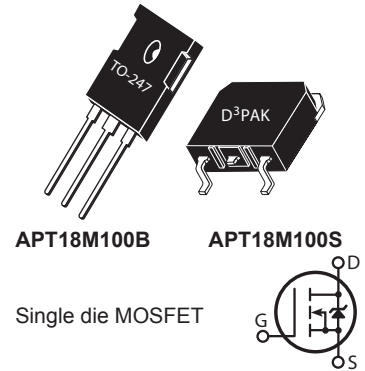
FEATURES

- **Fast switching with low EMI/RFI**
- **Low $R_{DS(on)}$**
- **Ultra low C_{rss} for improved noise immunity**
- **Low gate charge**
- **Avalanche energy rated**
- **RoHS compliant**

TYPICAL APPLICATIONS

- **PFC and other boost converter**
- **Buck converter**
- **Two switch forward (asymmetrical bridge)**
- **Single switch forward**
- **Flyback**
- **Inverters**

Absolute Maximum Ratings

Symbol	Parameter	Ratings	Unit
I_D	Continuous Drain Current @ T_C = 25°C	18	A
	Continuous Drain Current @ T_C = 100°C	12	
I_{DM}	Pulsed Drain Current [1]	68	
V_{GS}	Gate-Source Voltage	±30	V
E_{AS}	Single Pulse Avalanche Energy [2]	1070	mJ
I_{AR}	Avalanche Current, Repetitive or Non-Repetitive	9	A

Thermal and Mechanical Characteristics

Symbol	Characteristic	Min	Typ	Max	Unit
P_D	Total Power Dissipation @ T_C = 25°C			625	W
$R_{\theta JC}$	Junction to Case Thermal Resistance			0.20	°C/W
$R_{\theta CS}$	Case to Sink Thermal Resistance, Flat, Greased Surface		0.11		
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55		150	°C
T_L	Soldering Temperature for 10 Seconds (1.6mm from case)			300	
W_T	Package Weight		0.22		oz
			6.2		g
Torque	Mounting Torque (TO-247 Package), 6-32 or M3 screw			10	in·lbf
				1.1	N·m

Static Characteristics $\quad$ $T_J = 25°C$ unless otherwise specified $\quad$ APT18M100B_S

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
$V_{BR(DSS)}$	Drain-Source Breakdown Voltage	$V_{GS} = 0V$, $I_D = 250\mu A$		1000			V
$\Delta V_{BR(DSS)}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	Reference to 25°C, $I_D = 250\mu A$			1.15		V/°C
$R_{DS(on)}$	Drain-Source On Resistance ③	$V_{GS} = 10V$, $I_D = 9A$			0.60	0.70	Ω
$V_{GS(th)}$	Gate-Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 1mA$		3	4	5	V
$\Delta V_{GS(th)}/\Delta T_J$	Threshold Voltage Temperature Coefficient				-10		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 1000V$	$T_J = 25°C$			100	μA
		$V_{GS} = 0V$	$T_J = 125°C$			500	
I_{GSS}	Gate-Source Leakage Current	$V_{GS} = \pm30V$				±100	nA

Dynamic Characteristics $\quad$ $T_J = 25°C$ unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
g_{fs}	Forward Transconductance	$V_{DS} = 50V$, $I_D = 9A$		19		S
C_{iss}	Input Capacitance	$V_{GS} = 0V$, $V_{DS} = 25V$ $f = 1MHz$		4845		pF
C_{rss}	Reverse Transfer Capacitance			65		
C_{oss}	Output Capacitance			405		
$C_{o(cr)}$ ④	Effective Output Capacitance, Charge Related	$V_{GS} = 0V$, $V_{DS} = 0V$ to 667V		165		
$C_{o(er)}$ ⑤	Effective Output Capacitance, Energy Related			85		
Q_g	Total Gate Charge	$V_{GS} = 0$ to 10V, $I_D = 9A$, $V_{DS} = 500V$		150		nC
Q_{gs}	Gate-Source Charge			26		
Q_{gd}	Gate-Drain Charge			70		
$t_{d(on)}$	Turn-On Delay Time	**Resistive Switching** $V_{DD} = 667V$, $I_D = 9A$ $R_G = 4.7\Omega$⑥, $V_{GG} = 15V$		22		ns
t_r	Current Rise Time			20		
$t_{d(off)}$	Turn-Off Delay Time			75		
t_f	Current Fall Time			19		

Source-Drain Diode Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_S	Continuous Source Current (Body Diode)	MOSFET symbol showing the integral reverse p-n junction diode (body diode)			18	A
I_{SM}	Pulsed Source Current (Body Diode) ①				68	
V_{SD}	Diode Forward Voltage	$I_{SD} = 9A$, $T_J = 25°C$, $V_{GS} = 0V$			1.0	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 9A$ ③		1080		ns
Q_{rr}	Reverse Recovery Charge	$di_{SD}/dt = 100A/\mu s$, $T_J = 25°C$		24		μC
dv/dt	Peak Recovery dv/dt	$I_{SD} \leq 9A$, di/dt ≤1000A/μs, $V_{DD} = 800V$, $T_J = 125°C$			10	V/ns

① Repetitive Rating: Pulse width and case temperature limited by maximum junction temperature.

② Starting at $T_J = 25°C$, L = 26.42mH, $R_G = 4.7\Omega$, $I_{AS} = 9A$.

③ Pulse test: Pulse Width < 380μs, duty cycle < 2%.

④ $C_{o(cr)}$ is defined as a fixed capacitance with the same stored charge as C_{OSS} with $V_{DS} = 67\%$ of $V_{(BR)DSS}$.

⑤ $C_{o(er)}$ is defined as a fixed capacitance with the same stored energy as C_{OSS} with $V_{DS} = 67\%$ of $V_{(BR)DSS}$. To calculate $C_{o(er)}$ for any value of V_{DS} less than $V_{(BR)DSS}$, use this equation: $C_{o(er)} = -1.41E\text{-}8/V_{DS}^2 + 2.48E\text{-}9/V_{DS} + 4.81E\text{-}11$.

⑥ R_G is external gate resistance, not including internal gate resistance or gate driver impedance. (MIC4452)

Microsemi reserves the right to change, without notice, the specifications and information contained herein.
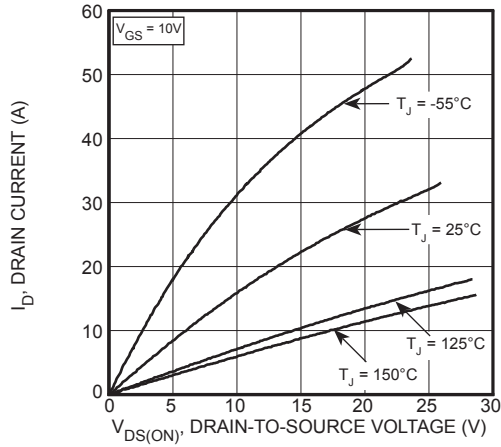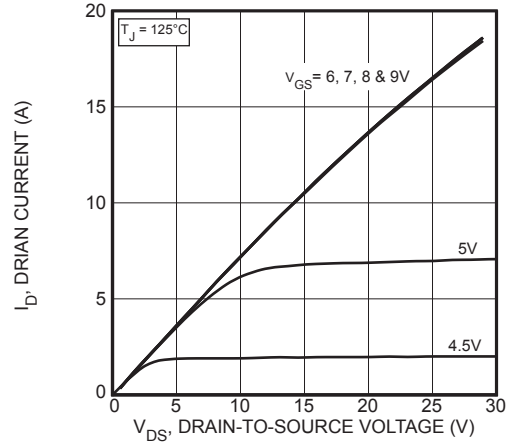
Figure 1, Output Characteristics
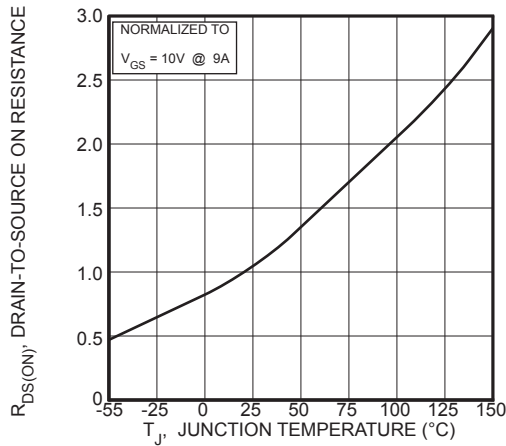

Figure 2, Output Characteristics

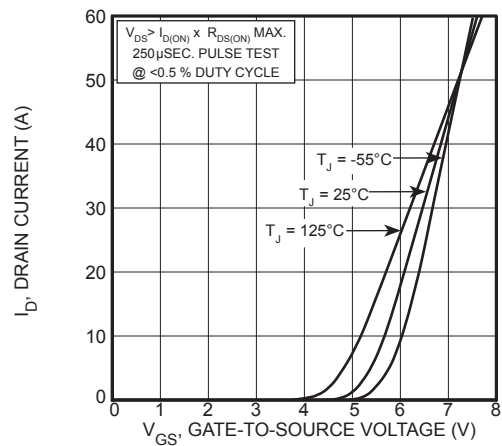**Figure 3, R_DS(ON) vs Junction Temperature**

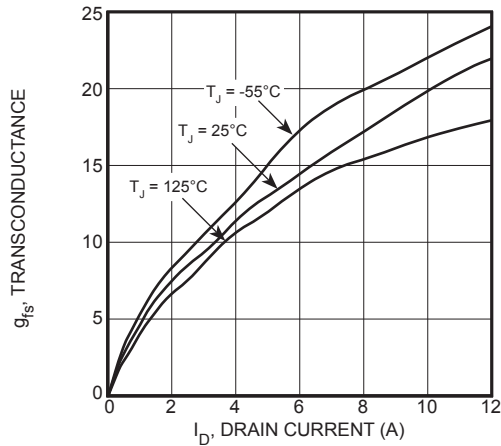**Figure 4, Transfer Characteristics**

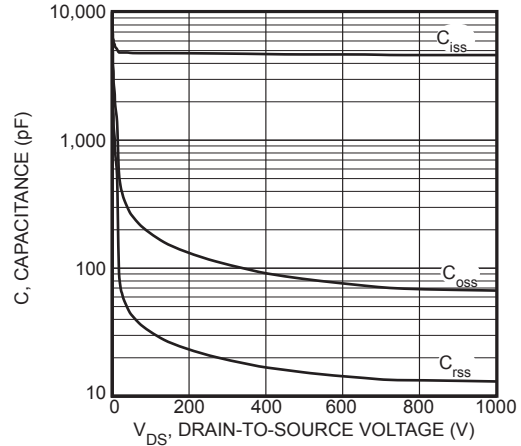

Figure 5, Gain vs Drain Current

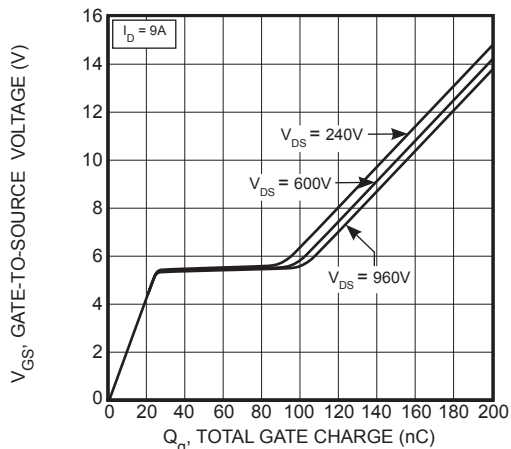**Figure 6, Capacitance vs Drain-to-Source Voltage**
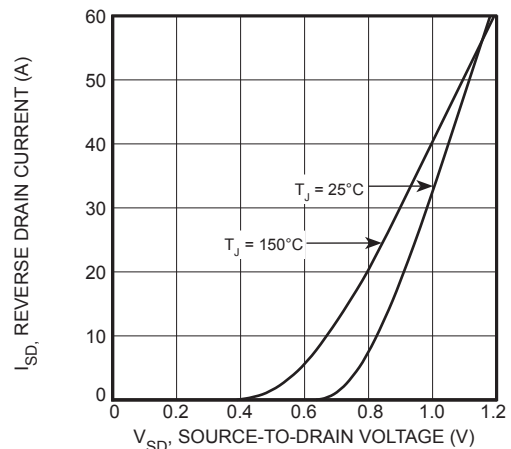

Figure 7, Gate Charge vs Gate-to-Source Voltage

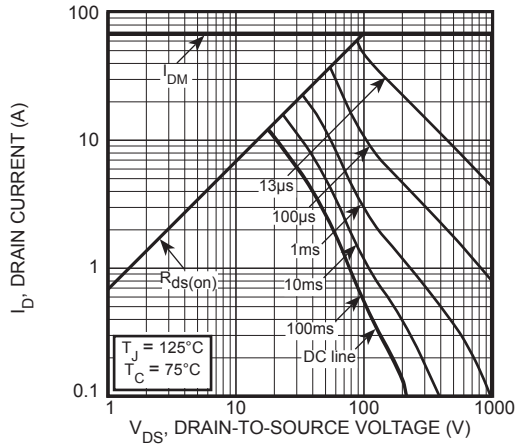**Figure 8, Reverse Drain Current vs Source-to-Drain Voltage**
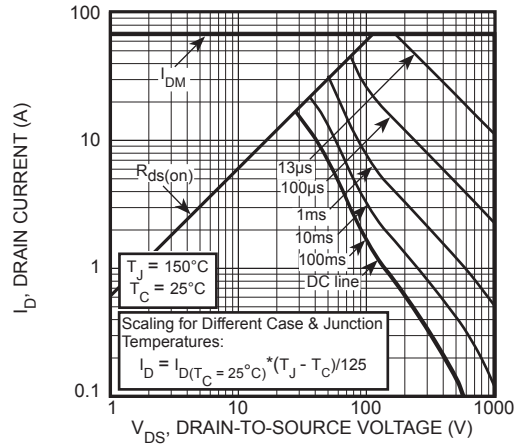
Figure 9, Forward Safe Operating Area

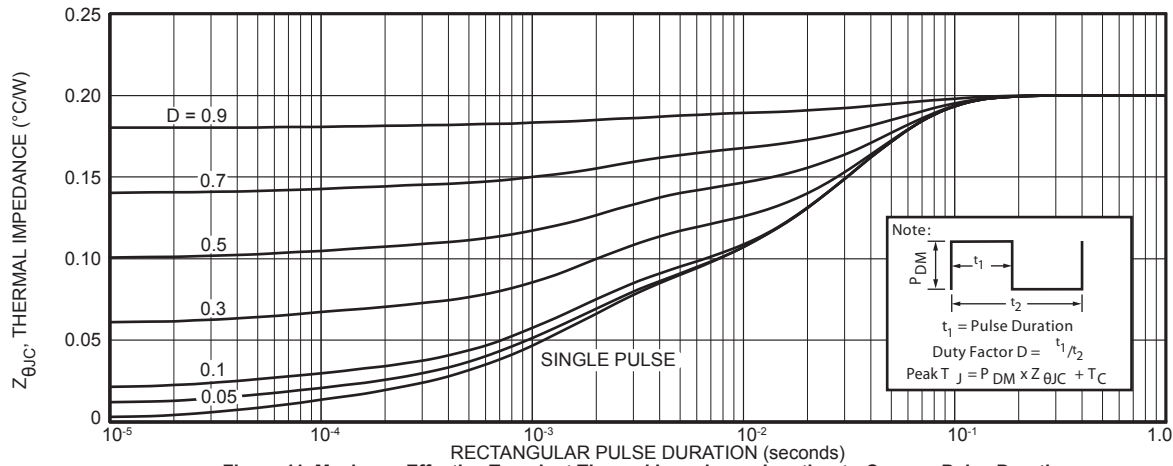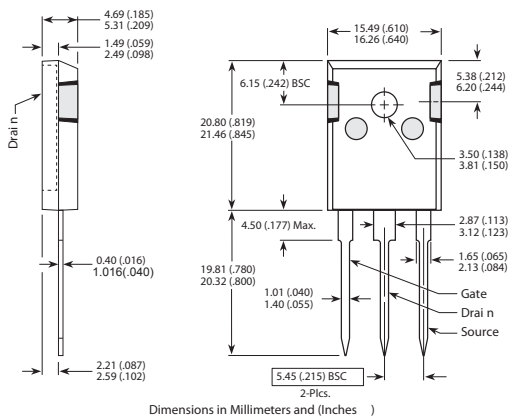**Figure 10, Maximum Forward Safe Operating Area**

Figure 11. Maximum Effective Transient Thermal Impedance Junction-to-Case vs Pulse Duration

TO-247 (B) Package Outline

Dimensions in Millimeters and (Inches)

D³PAK Package Outline

e3 100% Sn Plated

Dimensions in Millimeters (Inches)