



## 74HCT164

8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS

## Description

The 74HCT164 is a serial input 8-bit edge-triggered shift register that has outputs from each of eight stages.

### SERIAL DATA INPUT PINS

The serial input data is entered at pin SDA or pin SDB as these are logically ANDED. Either input could be used as an active HIGH enable with data entry on the other pin. If a single input is desired, the pins can be tied together or the unused input can be tied HIGH.

### DATA ENTRY

Data is shifted into Q0 from the serial input pins on each LOW to HIGH transition of the CP pin. Also, during the CP edge the data is transferred from each Qn to Qn+1. The serial data on pins DSA and DSB must be stable before and after the CP rising edge to meet the set-up and hold timing requirements.

#### RESET

When asserted LOW the Master Reset (MR) pin sets all Qn to LOW. This action does not depend on the condition of serial input or clock pins. The  $\overline{\text{MR}}$  must be asserted HIGH for a recovery time before the next CP positive edge pulse.

## **Features**

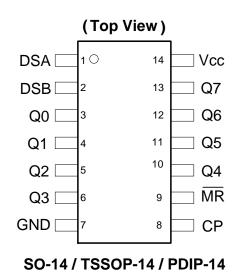
- Supply Voltage Range from 4.5V to 5.5V
- Sinks or Sources 4mA at V<sub>CC</sub> = 4.5V
- CMOS Low Power Consumption
- Schmitt Trigger Action at All Inputs
- TTL Compatible
- ESD Protection Exceeds JESD 22
  - 200-V Machine Model (A115)
  - 2000-V Human Body Model (A114)
  - Exceeds 1000-V Charged Device Model (C101)
- Range of Package Options SO-14 and TSSOP-14
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)

Notes: 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.

- 2. See http://www.diodes.com/quality/lead\_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Device ordering information is on page 7

## **Pin Assignments**



## Applications

- General Purpose Logic
  - Wide Array of Products Such as:
    - PCs, Networking, Notebooks, Netbooks
    - Computer Peripherals, Hard Drives, CD/DVD ROMs
    - TVs, DVDs, DVRs, Set-Top Boxes



# **Pin Descriptions**

Pin Number	Pin Name	Function	
1	DSA	Serial Data Input	
2	DSB	Serial Data Input	
3	Q0	Data Output	
4	Q1	Data Output	
5	Q2	Data Output	
6	Q3	Data Output	
7	GND	Ground	
8	CP	Clock Pulse – Positive Edge Triggered	
9	MR	Master Reset - Asynchronous	
10	Q4	Data Output	
11	Q5	Data Output	
12	Q6	Data Output	
13	Q7	Data Output	
14	V <sub>CC</sub>	Supply Voltage	

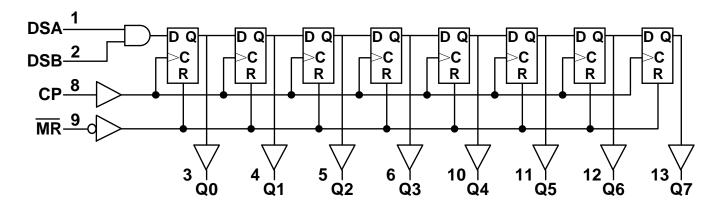
# **Function Table**

		In	Output			
Mode	MR	СР	DSA	DSB	Q0	Q1-Q7
Reset	L	Х	Х	Х	L	L
	н	<b>↑</b>	L	Х	L	Qn←Qn-1 (n= 1 to7)
Shift	н	<b>↑</b>	Х	L	L	Qn←Qn-1 (n= 1 to7)
	н	<u>↑</u>	Н	Н	Н	Qn←Qn-1 (n= 1 to7)

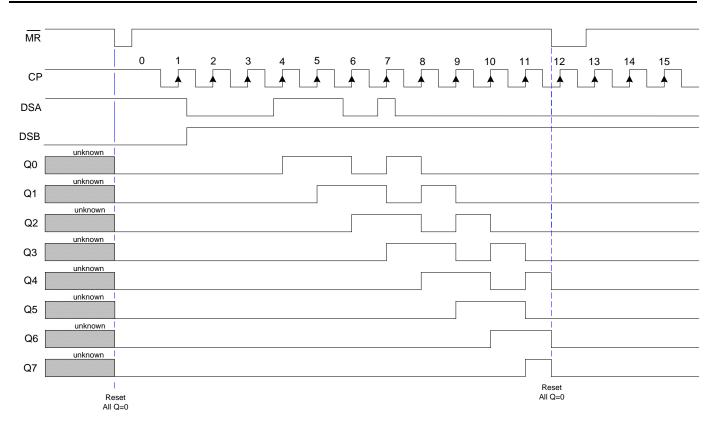
Note: 4. Signals asserted on DSA and DSB must be in place longer than Tsu (set up time) before CP occurs and remain in place Thold (hold time) after CP.



# Logic Diagram



# **Timing Diagram**



 Notes:
 5. All Q values are reset to LOW when MR goes low. MR is asynchronous and overrides all other signals.

 6. Serial data supplied at DSA and DSB is ANDED and transferred to Q0 on positive edge of CP.



## Absolute Maximum Ratings (Note 7) (T<sub>A</sub> = +25°C, unless otherwise specified.)

Symbol	Description	Rating	Unit
ESD HBM	Human Body Model ESD Protection	2	kV
ESD CDM	Charged Device Model ESD Protection	1	kV
ESD MM	Machine Model ESD Protection	200	V
V <sub>CC</sub>	Supply Voltage Range	-0.5 to +7.0	V
VI	Input Voltage Range (Note 8)	-0.5 to +7.0	V
I <sub>IK</sub>	Input Clamp Current VI < -0.5V or Vi > V <sub>CC</sub> +0.5V	±20	mA
Ι <sub>ΟΚ</sub>	Output Clamp Current $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$	±20	mA
lo	Continuous Output Current -0.5V < Vo V <sub>CC</sub> +0.5V	+/- 25	mA
Icc	Continuous Current Through Vcc	50	mA
I <sub>GND</sub>	Continuous Current Through GND	-50	mA
TJ	Operating Junction Temperature	-40 to +150	°C
T <sub>STG</sub>	Storage Temperature	-65 to +150	°C
PTOT	Total Power Dissipation	500	mW

7. Stresses beyond the absolute maximum may result in immediate failure or reduced reliability. These are stress values and device operation should Notes: be within recommend values.
 Input Voltage cannot exceed Vcc to the extent the Maximum clamp current is exceeded.

### Recommended Operating Conditions (Note 9) (T<sub>A</sub> = +25°C, unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	Supply Voltage	-	4.5	5.5	V
VI	Input Voltage	-	0	Vcc	V
Vo	Output Voltage	-	0	Vcc	V
Δt/ΔV	Input transition rise or fall rate	$V_{CC} = 4.5V$	-	140	ns/V
T <sub>A</sub>	Operating Free-Air Temperature	-	-40	+125	°C

Note: 9. Unused inputs should be held at  $V_{CC}$  or Ground.

# Electrical Characteristics (T<sub>A</sub> = +25°C, unless otherwise specified.)

Symbol	Parameter	Test Conditions	Vcc	Т	<sub>A</sub> = +25°C		T <sub>A</sub> = -4 +85		T <sub>A</sub> = -40°C	to +125°C	Unit
•		Conditions		Min.	Тур.	Max.	Min.	Max.	Min.	Max.	
VIH	High-Level Input Voltage	-	4.5V to 5.5V	2.0	1.6	-	2.0	-	2.0	-	V
VIL	Low-Level Input Voltage	-	4.5V to 5.5V	-	1.2	0.8	-	0.8	-	0.8	V
	High-Level	I <sub>OH</sub> = -20µА 4.5∖	4.5V	4.4	4.5	-	4.4	-	4.4	-	v
Vон	Output Voltage	I <sub>OH</sub> = -4.0mA	4.5V	3.98	4.32	-	3.84	-	3.7	-	v
N/	Low-level	I <sub>OL</sub> = 20μΑ	4.5V	-	0	0.1	-	0.1	-	0.1	v
V <sub>OL</sub>	Output Voltage	$I_{OL} = 4mA$	4.5V	-	0.15	0.26	-	0.33	-	0.4	v
I <sub>I</sub>	Input Current	V <sub>I</sub> =GND or Vcc	6.0V	-	-	±0.1	-	± 1	-	± 1	μA
Icc	Supply Current	$V_I = GND \text{ or}$ $V_{CC}, I_O = 0$	6.0V	-	-	8.0	-	80	-	160	μA
Δlcc	Additional Supply Current	$V_{I}=V_{CC}-2.1V$ $I_{O} = 0$ Other inputs at $V_{CC}$ or GND.	4.5V to 5.5V	-	100	360	-	450	-	490	μA



# **Switching Characteristics**

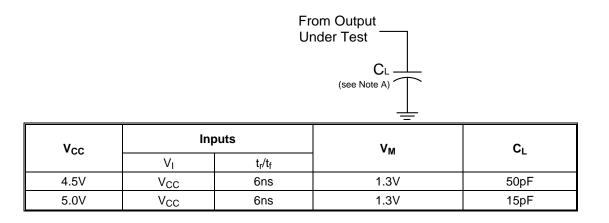
Symbol /		Test			T <sub>A</sub> = +25°C		-40°C to	+85°C	-40°C to	o +125℃	Unit
Parameter	Pins	Conditions	Vcc	Min	Тур.	Max	Min	Max	Min	Max	
f <sub>MAX</sub>	СР	Figure 1	4.5V	27	55	-	22	-	18	-	MHz
Maximum	0	r igure i	5.0V	-	61	-	-	-	-	-	
t <sub>w</sub> Pulse Width	CP HIGH or LOW	Figure 1	4.5V	18	7	-	23	-	27	-	ns
	MR LOW	Figure 1	4.5V	18	10	-	23	-	27	-	ns
t <sub>s∪</sub> Set-up Time	DSA or DSB to CP	Figure 1	4.5V	12	6	-	15	-	18	-	ns
t <sub>H</sub> Hold Time	DSA or DSB to CP	Figure 1	4.5V	4	-2	-	4	-	4	-	ns
t <sub>rec</sub> Recovery Time	MR to CP	Figure 1	4.5V	16	7	-	20	-	24	-	ns-
t <sub>PD</sub>		Figure 1	4.5V	-	17	36	-	45	-	54	
Propagation	CP to Qn		5.0V	-	14		-		-		ns
t <sub>PHL</sub>		Figure 1	4.5V	-	19	38	-	48	-	57	
HIGH to LOW Propagation	MR to Qn		5.0V	-	16	-	-	-	-	-	ns
t <sub>⊤</sub> Transition Time	All Signals	Figure 1	4.5V	-	7	15	-	19	-	22	ns

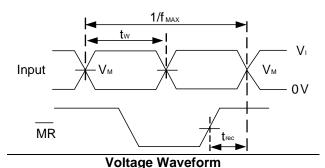
# **Operating Characteristics** (T<sub>A</sub> = +25°C, unless otherwise specified.)

	Parameter	Test Conditions	V <sub>CC</sub> = 6V Typ	Unit
C <sub>pd</sub>	Power Dissipation Capacitance per Gate	f = 1 MHz V <sub>I</sub> = Gnd to Vcc-1.5V	40	pF
Cı	Input Capacitance	V <sub>I</sub> = Gnd or Vcc	3.5	pF

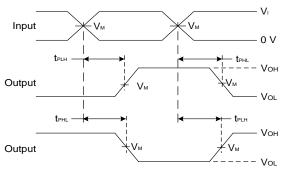


## **Parameter Measurement Information**





Pulse Duration and Recovery Time

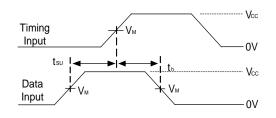


### Voltage Waveform Propagation Delay Times Inverting and Non Inverting Outputs

Notes: A . Includes test lead and test apparatus capacitance.

- B. All pulses are supplied at pulse repetition rate ≤10 MHz
- C. Inputs are measured separately one transition per measurement
- D.  $t_{\text{PLH}}$  and  $t_{\text{PHL}}$  are the same as  $t_{\text{PD}}$
- E. Transition times  $t_t$   $t_{th}$ ,  $t_{th}$ ,  $t_{th}$  are measured from the 10% to 90% or 90% to 10% of the appropriate waveform.

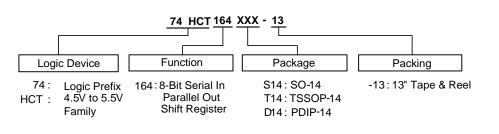
### Figure 1 Load Circuit and Voltage Waveforms



Voltage Waveform Set-up and Hold Times



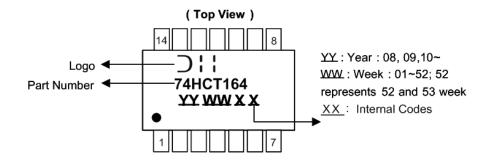
# **Ordering Information**



Device	Package Code	Packaging	Pac	king
Device	Fackage Code	Fackaying	Quantity	Part Number Suffix
74HCT164S14-13	S14	SO-14	2,500/Tape & Reel	-13
74HCT164T14-13	T14	TSSOP-14	2,500/Tape & Reel	-13
74HCT164D14	D14	PDIP-14	Tube	-

# **Marking Information**

### (1) SO-14, TSSOP-14, PDIP-14



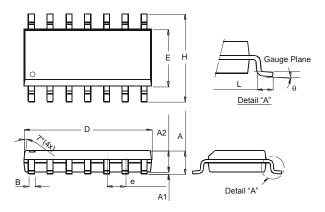
Part Number	Package
74HCT164S14-13	SO-14
74HCT164T14-13	TSSOP-14
74HCT164D14	PDIP-14



# Package Outline Dimensions (All dimensions in mm.)

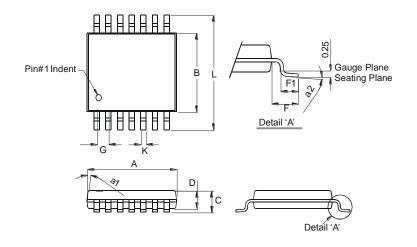
Please see AP02002 at http://www.diodes.com/datasheets/ap02002.pdf for the latest version.

### Package Type: SO-14



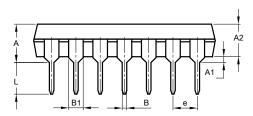
	SO-14					
Dim	Min	Max				
Α	1.47	1.73				
A1	0.10	0.25				
A2	1.45	Тур				
В	0.33	0.51				
D	8.53	8.74				
Е	3.80	3.99				
е	1.27	Тур				
Н	5.80	6.20				
L	0.38	1.27				
θ	0°	8°				
All Di	mension	s in mm				

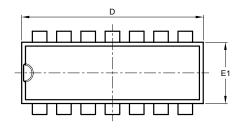
### Package Type: TSSOP-14

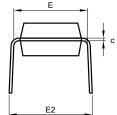


	TSSOP-1	4			
Dim	Min	Max			
a1	7° (	4X)			
a2	0°	8°			
Α	4.9	5.10			
В	4.30	4.50			
С	_	1.2			
D	0.8	1.05			
F	1.00	Тур			
F1	0.45	0.75			
G	0.65	Тур			
K	0.19	0.30			
L	L 6.40 Typ				
All Dir	nensions				

Package Type: PDIP-14







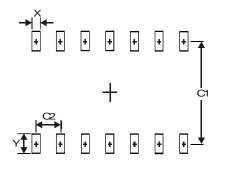
	PDIP-14					
Dim	Min	Max				
Α	3.710	4.310				
A1	0.510	-				
A2	3.200	3.600				
В	0.380	0.570				
B1	1.524 (BSC)					
c	0.204	0.360				
D	18.800	19.200				
ш	6.200	6.600				
E1	7.320	7.920				
E2	8.400	9.000				
e	2.540 (BSC)					
L	3.000	3.600				
All D	imensions	in mm				



## **Suggested Pad Layout**

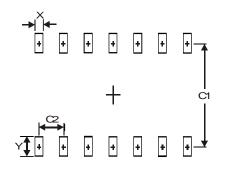
Please see AP02001 at http://www.diodes.com/datasheets/ap02001.pdf for the latest version.

#### Package Type: SO-14



Dimensions	Value (in mm)
Х	0.60
Y	1.50
C1	5.4
C2	1.27

Package Type: TSSOP-14



Dimensions	Value (in mm)
Х	0.45
Y	1.45
C1	5.9
C2	0.65



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